US005590342A

[11] **Patent Number: 5,590,342**

[45] **Date of Patent: Dec. 31, 1996**

[57] **ABSTRACT**

A power management mechanism for use in a computer system having a bus, a memory for storing data and instructions, and a central processing unit (CPU). The CPU runs an operating system having a power management virtual device driver (PMVxD) responsible for performing idle detection for devices. The PMVxD performs idle detection using event timers that provide an indicator as to the activity level. The PMVxD places idle local devices in a reduced power consumption state when no activity has occurred for a predetermined period of time.

35 Claims, 7 Drawing Sheets